AMENDMENTS TO THE CLAIMS

1. (Original) A method comprising:

receiving a multiple-data load instruction;

executing the multiple-data load instruction; and

loading, in response to execution of the multiple-data load instruction, data within a destination data storage device, wherein one or more data elements from the data are randomly located within a source memory device.

2. (Original) The method of claim 1, wherein loading data further comprises:

receiving a source value indicating the memory device wherein the data is located;

receiving a device value indicating an address storage device containing addresses of the data elements;

reading, from the memory device, a data element for each address within the address storage device;

receiving a destination value indicating the destination data storage device wherein to load the data elements; and

storing each data element read from the memory device into the destination data storage device.

3. (Currently Amended) The method of claim 2, wherein reading the data ~~elements~~ element further comprises:

receiving a table value indicating a look-up table within the memory device wherein the data elements are initially stored;

receiving an offset value indicating a data region within a respective look-up table wherein the data elements are initially stored;

selecting an address index from the address data storage device;

reading a data element from the data region of the look-up table according to the selected address index; and

repeating the selecting and reading from each address index within the address data storage device.

4. (Currently Amended) The method of claim 2, wherein reading a data ~~elements~~ element further comprises:

receiving a memory access data type value indicating a data type of the data;

receiving a base address value indicating a start location of a data storage area within the memory device wherein the data elements are initially stored;

receiving an offset value indicating a data region within the data storage area wherein the data elements are initially stored;

selecting an address index from the address data storage device;

when a multiply value is received, setting the selected address index equal to the selected address index multiplied by the multiply value according to the data type of the data;

reading a data element from the data region of the data storage area according to the selected address index; and

repeating the selecting and reading from each address index within the address data storage device.

5. (Original) The method of claim 4, further comprising:

receiving an address index data type, indicating a data type of the address indexes within the address storage device as one of a byte data type, a word data type and a double word data type.

6. (Original) The method of claim 4, wherein the memory access data type is one of a byte data type, a word data type and a double word data type.

7. (Currently Amended) The method of claim ~~1~~2, wherein receiving a destination value further comprises:

receiving, for one or more data elements, an address location within the destination data storage device wherein to store a respective data element.

8. (Original) The method of claim 1, wherein addresses of the data elements are stored within an address data storage device, and prior to loading the data, the method further comprises:

organizing, in response to executing a data shuffle instruction, address elements within the address data storage device according to a data processing operation.

9. (Original) The method of claim 1, further comprising:

organizing, in response to executing a data shuffle instruction, data elements within the destination data storage device according to a data processing operation.

10. (Original) The method of claim 1, further comprising:

processing, in response to executing a data processing instruction, data elements within the destination data storage device according to the data processing instruction.

11. (Currently Amended) A machine readable storage medium including program instructions that direct a system to function in a specified manner when executed by a processor, the program instructions comprising:

loading, in response to execution of a multiple-data load instruction, data ~~within~~ from at least one data storage area of a memory device to a destination data storage device, wherein one or more data elements from the data are randomly located within ~~a source~~the memory device.

12. (Original) The machine readable storage medium of claim 11, wherein loading data further comprises:

receiving a source value indicating the memory device wherein the data is located;

receiving a device value indicating an address data storage device containing addresses of the data elements;

reading, from the memory device, a data element for each address within the address storage device;

receiving a destination value indicating the destination data storage device wherein to load the data elements; and

storing each data element read from the memory device into the destination data storage device.

13. (Currently Amended) The machine readable storage medium of claim 12, wherein reading a data ~~elements~~ element further comprises:

receiving a table value indicating a look-up table within the memory device wherein the data elements are initially stored;

receiving an offset value indicating a data region within a respective look-up table wherein the data elements are initially stored;

selecting an address index from the address data storage device;

reading a data element from the data region of the look-up table according to the selected address index; and

repeating the selecting and reading from each address index within the address data storage device.

14. (Currently Amended) The machine readable storage medium of claim 12, wherein reading a data ~~elements~~ element further comprises:

receiving a memory access data type value indicating a data type of the data;

receiving a base address value indicating a start location of a data storage area within the memory device wherein the data elements are initially stored;

receiving an offset value indicating a data region within a respective data storage area wherein the data elements are initially stored;

selecting an address index from the address storage device;

when a multiply value is received, setting the selected address index equal to the selected address index multiplied by the multiply value according to the data type of the data;

reading a data element from the data region of the data storage area according to the selected address index; and

repeating the selecting and reading from each address index within the address data storage device.

15. (Original) The machine readable storage medium of claim 14, further comprising:

receiving an address index data type, indicating a data type of the address indexes within the address storage device as one of a byte data type, a word data type and a double word data type.

16. (Original) The machine readable storage medium of claim 14, wherein the memory access data type is one of a byte data type, a word data type and a double word data type.

17. (Currently Amended) The machine readable storage medium of claim ~~11~~12, wherein receiving a destination value further comprises:

receiving, for one or more data elements, an address location within the destination data storage device wherein to store a respective data element.

18. (Original) The machine readable storage medium of claim 11, wherein addresses of the one or more data elements are stored within an address data storage device, and prior to loading the data, the method further comprises:

organizing, in response to executing a data shuffle instruction, address elements within the address data storage device according to a data processing operation.

19. (Original) The machine readable storage medium of claim 11, further comprising:

organizing, in response to executing a data shuffle instruction, data elements within the destination data storage device according to a data processing operation.

20. (Original) The machine readable storage medium of claim 11, further comprising:

processing, in response to executing a data processing instruction, data element within the destination data storage device according to the data processing instruction.

21. (Currently Amended) An apparatus, comprising:

a processor having ~~circuitry to~~an execution unit to execute instructions;

a memory device including one or more data storage areas to contain~~ing~~ data generated during apparatus initialization;

~~an address data storage device~~a register file coupled to the processor, ~~the~~ including an address data storage device including address indexes of data elements within a respective data storage ~~are~~ area within the memory device; and

~~a storage device coupled to the processor, having sequences of instructions stored therein, which when executed by the processor cause the processor to:~~

the execution unit to load, in response to execution of a multiple-data load instruction, data ~~within~~ from the one or more data storage areas of the memory device to a destination data storage device, wherein one or more data elements from the data are randomly ~~located~~ stored within the memory device.

22. (Currently Amended) The apparatus of claim 21, ~~wherein the instruction to load data~~ further ~~causes the processor to~~comprising:

a storage device coupled to the processor, having sequences of instructions stored therein, which when executed by the execution unit cause the processor to:

generate data elements according to a data generation instruction; and

store the data elements within the one or more data storage areas of the memory device.

23. (Currently Amended) The apparatus of claim 21, wherein the multiple data load instruction ~~to load data~~ further causes the ~~processor~~ execution unit to:

select a data storage area within the memory device based on a received data storage area value;

calculate a location of a respective data element within the selected data storage area;

read the respective data element from the calculated location; and

store the respective data element within the destination data storage device.

24. (Currently Amended) The apparatus of claim 23, wherein the instruction to store the respective data further causes the ~~processor~~ execution unit to:

store the respective data element at a received address location within the destination data storage device.

25. (Currently Amended) The apparatus of claim 23, wherein the instruction to calculate the location of the respective data element further causes the ~~processor~~ execution unit to:

receive a device value indicating an address storage device containing the addresses of the data elements;

receive a table value indicating a look-up table within the memory device wherein the data elements are initially stored; and

receive an offset value indicating a data region within a respective look-up table, wherein the data elements are initially stored such that the location of the respective data element is calculated as an address index of the respective data element within the look-up table.

26. (Currently Amended) The apparatus of claim 23, wherein instruction to calculate the location of the respective data element further causes the ~~processor~~ execution unit to:

receive a memory access data type value indicating a data type of the data;

receive a base address value indicating a start location of a data storage area within the memory device wherein the data elements are initially stored;

receive a device value indicating an address storage device containing the addresses of the data elements including a multiply value indicating a value which is multiplied to address indexes within the address data storage device according to the memory access data type of the data;

receive an offset value indicating a data region within a respective data storage area, wherein the data elements are initially stored such that the location of the respective data element is calculated as an address index of the respective data element within the data region.

27. (Currently Amended) The apparatus of claim 21, further comprising:

a data shuffle unit coupled between the register file and the execution unit, the data shuffle unit to organize, in response to execution of ~~a n~~an address shuffle instruction, address elements within the address data storage device according to a data processing operation and to organize, in response to executing a data shuffle instruction, data elements within the destination data storage device according to a data processing operation.

Please add the following new claim:

-- 28. (New) A system comprising:

a processor having an execution unit to execute instructions;

a memory device including one or more data storage areas to store data generated during application initialization;

a register file coupled to the execution unit, including an address data storage device including address indices of data elements within a respective data storage area of the memory device;

a data shuffle unit coupled between the register file and the execution unit, the data shuffle unit to organize, in response to execution of an address shuffle instruction, address elements within the address data storage device according to a data processing operation and to

organize, in response to executing a data shuffle instruction, data elements within the destination data storage device according to a data processing operation; and

the execution unit to load, in response to execution of a multiple data load instruction, data from at least one data storage area of the memory device to the destination data storage device, wherein one or more data elements from the data are randomly stored within the memory device. --